**REMARKS**

This Amendment responds to the Office Action dated October 27, 2009 in which the Examiner rejected claims 1-3, 7, 11-13, 17, 21-23, 27, 31-33, 37, 41-43 and 47 under 35 U.S.C. § 102 (e) and rejected claims 4-6, 8-10, 14-16, 18-20, 24-26, 28-30, 34-36, 38-40, 44-46 and 48-50 under 35 U.S.C. § 103.

As indicated above, claims 1, 2, 8, 10-12, 18, 20-21, 31 and 41 have been amended in order to make explicit what is implicit in the claims. The amendment is unrelated to a statutory requirement for patentability.

As indicated above, claims 19, 22, 28-30, 32, 38-40, 42 and 48-50 have been amended to conform to the amendments made to the independent claims. The amendments are unrelated to a statutory requirement for patentability and do not narrow the literal scope of the claims.

Claims 1-2, 8, 10, 21 and 31 claim a multiplexing apparatus and claims 11-12, 18, 20 and 41 claim a multiplexing method. The multiplexing apparatus and method multiplex audio and video data using an instruction set stored in a memory. The claimed invention thus provides a multiplexing apparatus and method which reduces the processing burden on a CPU since the CPU does not have to transfer an instruction directly to a multiplexer at the time of transfer, but instead, the multiplex stream is generated by reading the instruction set from the memory. The prior art does not show, teach or suggest the invention as claimed in claims 1-2, 8, 10-12, 18, 20-21, 31 and 41.

Claims 1-3, 7, 11-13, 17, 21-23, 27, 31-33, 37, 41-43 and 47 were rejected under 35 U.S.C. § 102 (e) as being anticipated by *Robinett, et al.* (U.S. Publication No. 2002/0126711).

*Robinett, et al.* appears to disclose each descriptor is used to record a receipt time stamp, indicating when a transport packet is received at an input port, or a dispatch time stamp,

indicated the time at which a transport packet is to be transmitted from an output port. For transport packets received at an input port, a data link control circuit records a receipt time stamp in the descriptor allocated to each received and retained transport packet indicating a time at which the transport packet was received. The descriptors are maintained in order of receipt in the receipt queue. In the case of outputting transport packets from an output port, the data link control circuit sequentially retrieves each descriptor from the transmit queue, and the transport packet to which each retrieved descriptor points. At a time corresponding to a dispatch time recorded in each retrieved descriptor, the data link control circuit transmits the retrieved transport packet to which each retrieved descriptor points in a time slot of the outputted transport stream corresponding to the dispatch time recorded in the retrieved descriptor [0037].

Thus, *Robinett, et al.* merely discloses a descriptor recording a time stamp indicating when a transport packet is received or a dispatch time stamp indicating the time at which a transport packet is to be transmitted. Nothing in *Robinett, et al.* shows, teaches or suggests calculating an order of multiplexing based on storage locations (supplied by encoders) as claimed in claims 1-2, 11-12, 21, 31 and 41. Rather, *Robinett, et al.* merely discloses a descriptor recording a receipt time stamp or a dispatch time stamp.

Furthermore, *Robinett, et al.* merely discloses a data link control circuit sequentially retrieves each descriptor from the transmit queue and transport package to which the descriptor points and transmitting the transport packet in a time slot corresponding to the dispatched time recorded in the descriptor. Thus, nothing in *Robinett, et al.* shows, teaches or suggests generating an instruction set which describes the storage location and (calculated) order of multiplexing as claimed in claims 1-2, 11-12, 21, 31 and 41. Rather, *Robinett, et al.* only

discloses retrieving transport packets and dispatching them based upon a dispatch time recorded in a descriptor.

Additionally, *Robinett, et al.* appears to disclose receiving TS1 at a first adapter 110, receiving TS2 at a second adapter 110 and transmitting TS3 from a third adapter 110 of the same multiplexing mode 100 [0093]. The data link control circuit 112 sequentially retrieves from the cache 114 each descriptor in the transmit queue, in the order from the head pointer 124-3 and the transport packet in the transport packet storage location to which the descriptor points. When the time of the reference clock generator 113 of the third adaptor 1110 equals the time indicated in the dispatched time field 129-5 of the retrieved descriptor, the data link control circuit 1112 transmits the transport packet [0144].

Thus, *Robinett, et al.* merely discloses transmitting the transport packet when the clock generator 113 equals the time indicated in the dispatch time field of the retrieved descriptor. Nothing in *Robinett, et al.* shows, teaches or suggests reading the instruction set from a memory and generating a multiplexed stream by reading the data units from the memory in a predetermined order based on the instruction set as claimed in claims 1-2, 11-12, 21, 31 and 41. Rather, *Robinett, et al.* merely discloses transmitting the transport packet based upon the time generated by the clock generator and the time stored in the time field of the descriptor.

Since nothing in *Robinett, et al.* shows, teaches or suggests (a) calculating an order of multiplexing based on storage location, (b) generating an instruction set describing the storage location and (calculated) order of multiplexing and (c) reading the instruction set and generating a multiplex streamed by reading data units in a predetermined order based on the instruction set as claimed in claims 1-2, 11-12, 21, 31 and 41, Applicant respectfully requests the Examiner withdraws the rejection to claims 1-2, 11-12, 21, 31 and 41 under 35 U.S.C. § 102 (e).

Claims 3, 7, 13, 17, 22-23, 27, 32-33, 37, 42-43 and 47 recite additional features. Applicant respectfully submits that claims 3, 7, 13, 17, 22-23, 27, 32-33, 37, 42-43 and 47 would not have been anticipated by *Robinett, et al.* within the meaning of 35 U.S.C. § 102 (e) at least for the reasons as set forth above. Therefore, Applicant respectfully requests the Examiner withdraws the rejection to claims 3, 7, 13, 17, 22-23, 27, 32-33, 37, 42-43 and 47 under 35 U.S.C. § 102 (e).

Claims 8-9, 18-19, 28-29, 38-39 and 48-49 were rejected under 35 U.S.C. § 103 as being unpatentable over *Robinett, et al.* and further in view of *Dobson, et al.* (U.S. Patent No. 6,188,703).

As discussed above, *Robinett, et al.* only discloses transmitting a transport packet based upon a time stored in a descriptor. Nothing in *Robinett, et al.* shows, teaches or suggests (a) calculating an order of multiplexing based on storage location, (b) generating an instruction set describing storage location and (calculated) order of multiplexing and (c) reading the instruction set and generating a multiplexed stream by reading the data units in a predetermined order based upon the instruction set as claimed in claims 8 and 18. Rather, *Robinett, et al.* merely discloses transmitting a transport packet based upon a stored dispatch time.

*Dobson, et al.* appears to discloses a FIFO buffer 32 which signals a MUX microprocessor 22 when sufficient video data is in a buffer 32 (column 3, line 65-column 4, line 3). When a start code is detected, the value of the FIFO-fullness-counter 40 is latched into another counter called the start-code position counter 48. The start-code position counter 48 only counts down on compressed data FIFO read by the MUX 30 (column 4, lines 31-35).

Thus, *Dobson, et al.* merely discloses a buffer 32 which signals a microprocessor 22 when sufficient video data is in the buffer. Nothing in *Dobson, et al.* shows, teaches or suggests

(a) calculating an order of multiplexing based on storage locations, (b) generating an instruction set describing the storage location and (calculated) order of multiplexing and (c) reading the instruction set and generating a multiplexed stream by reading the data units in a predetermined order based upon the instruction set as claimed in claims 8 and 18. Rather, *Dobson, et al.* only discloses a buffer 32 signaling a microprocessor 22 when it is filled with sufficient data.

Additionally, *Dobson, et al.* merely discloses latching a value in a counter 40 when a start code is detected. Nothing in *Dobson, et al.* shows, teaches or suggests (a) calculating an order of multiplexing based on storage locations, (b) generating an instruction set describing the storage location and (calculated) order of multiplexing and (c) reading the instruction set and generating a multiplexed stream by reading the data units in a predetermined order based on the instruction set as claimed in claims 8 and 18. Rather, *Dobson, et al.* merely discloses latching a value when a start code is detected.

A combination of *Robinett, et al.* and *Dobson, et al.* would merely suggest to output a transport stream when the dispatch time stored in a descriptor is indicated by a clock generator as taught by *Robinett, et al.* and to signal when sufficient data is in a buffer as taught by *Dobson, et al.* Thus, nothing in the combination of the references shows, teaches or suggests (a) calculating and order of multiplexing based on storage location, (b) generating an instruction set describing the storage location and (calculated) order of multiplexing and (c) reading the instruction set and generating a multiplexed stream by reading the data units in a predetermined unit based on the instruction set as claimed in claims 8 and 18. Therefore, Applicant respectfully requests the Examiner withdraws the rejection to claims 8 and 18 under 35 U.S.C. § 103.

Claims 9, 19, 28-29, 38-39 and 48-49 recite additional features. Applicant respectfully submits that claims 9, 19, 28-29, 38-39 and 48-49 would not have been obvious within the

meaning of 35 U.S.C. § 103 over *Robinett, et al.* and *Dobson, et al.* at least for the reasons as set forth above. Therefore, Applicant respectfully requests the Examiner withdraws the rejection to claims 9, 19, 28-29, 38-39 and 48-49 under 35 U.S.C. § 103.

Claims 10, 20, 30, 40 and 50 were rejected under 35 U.S.C. § 103 as being unpatentable over *Robinett, et al.* in view of *Zaun, et al.* (U.S. Publication No. 2001/0024456).

As discussed above, nothing in *Robinett, et al.* shows, teaches or suggests (a) calculating an order of multiplexing based on storage location, (b) generating an instruction set describing the storage location and (calculated) order of multiplexing and (c) generating a multiplexed stream by reading data units in a predetermined order based on the instruction set as claimed in claims 10 and 20. Rather, *Robinett, et al.* merely discloses transmitting a transport stream based upon a dispatch time stored in a descriptor.

*Zaun, et al.* appears to disclose a remultiplexing module including an output processor 124 which generates two or more output streams from data stored in packet buffers 104. The output processing section then generates two or more independent high-speed transport multiplex output streams incorporating the selected packet data [0035].

Thus, *Zaun, et al.* merely discloses outputting two or more multiplexed streams. Nothing in *Zaun, et al.* shows, teaches or suggests (a) calculating an order of multiplexing based on storage location, (b) generating an instruction set which describes the storage location and (calculated) order of multiplexing and (c) generating the multiplexed stream by reading the data units in a predetermined order based upon the read instruction set as claimed in claims 10 and 20. Rather, *Zaun, et al.* merely discloses outputting two or more multiplexed streams.

A combination of *Robinett, et al.* and *Zaun, et al.* would merely suggest to output a transport stream based upon an obtained time stamp as taught by *Robinett, et al.* and to generate

two or more output streams as taught by *Zaun, et al.* Thus, nothing in the combination of the references shows, teaches or suggests (a) calculating an order of multiplexing based on storage location, (b) generating an instruction set describing the storage location and (calculated) order of multiplexing and (c) generating the multiplexed stream by reading data units in a predetermined order based on the read instruction set as claimed in claims 10 and 20. Therefore, Applicant respectfully requests the Examiner withdraws the rejection to claims 10 and 20 under 35 U.S.C. § 103.

Claims 30, 40 and 50 recite additional features. Applicant respectfully submits that claims 30, 40 and 50 would not have been obvious within the meaning of 35 U.S.C. § 103 over *Robinett, et al.* and *Zaun, et al.* at least for the reasons as set forth above. Therefore, Applicant respectfully requests the Examiner withdraws the rejection to claims 30, 40 and 50 under 35 U.S.C. § 103.

Claims 4-6, 14-16, 24-26, 34-36 and 44-46 were rejected under 35 U.S.C. § 103 as being unpatentable over *Robinett, et al.* in view of *Kelly, et al.* (U.S. Publication No. 2001/0036355).

Applicant respectfully traverses the Examiner's rejection of the claims under 35 U.S.C. § 103. The claims have been reviewed in light of the Office Action, and for reasons which will be set forth below, Applicant respectfully requests the Examiner withdraws the rejection to the claims and allows the claims to issue.

As discussed above, since nothing in *Robinett, et al.* shows, teaches or suggests the primary features as claimed in claims 1, 12, 21, 31 and 41 as discussed above, Applicant respectfully submits that the combination of the primary reference with the secondary reference to *Kelly, et al.* would not overcome the deficiencies of the primary reference. Therefore,

Applicant respectfully requests the Examiner withdraws the rejection to claims 4-6, 14-16, 24-26, 34-36 and 44-46 under 35 U.S.C. § 103.

Thus, it now appears that the application is in condition for a reconsideration and allowance. Reconsideration and allowance at an early date are respectfully requested. Should the Examiner find that the application is not now in condition for allowance, Applicant respectfully requests the Examiner enters this Amendment for purposed of appeal.

## CONCLUSION

If for any reason the Examiner feels that the application is not now in condition for allowance, the Examiner is requested to contact, by telephone, the Applicant's undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed within the currently set shortened statutory period, Applicant respectfully petitions for an appropriate extension of time. The fees for such extension of time may be charged to Deposit Account No. 50-0320.

In the event that any additional fees are due with this paper, please charge to our Deposit Account No. 50-0320.

Respectfully submitted,

FROMMER LAWRENCE & HAUG LLP
Attorneys for Applicant

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By_____
Ellen Marcie Emas
Reg. No. 32,131
(202) 292-1530